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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,200	06/27/2003	Shion-Hau Liaw	3313-1009P	5799

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,200	LIAW ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

Information Disclosure Statement (IDS) filed on 10/31/03 was considered.

2. Claims 1-16 are presented for examination.

Specification

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed

Claim Rejections - 35 USC ∋ 112

4. Claim 2-8, 12-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There are insufficient antecedent basis for the limitations.

In claim 2-7 and 12-15recite the limitation of:

"the voltage"

"the control gate"

"the split-gate transistors"

In claim 8 and 16 recite the limitation of:

"the voltage"

"the word line"

Claim Rejections - 35 USC ∋ 112

5. Claim 4 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is vague and not clear, therefore can not be understood by the examiner if the specific claimed voltages applied to the control gates and the sources of the split-gate transistors is applied to which operation (an erase, reading or program operation?) of the device.

Claim Rejections - 35 USC ∋ 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-2 and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ratnakumar et al, Pat. No. 6556487.

With regard to claim 1, Ratnakumar discloses a non-volatile static random access memory (SRAM) cell, comprising: an SRAM unit (fig. 8, 310), which receives a 1-bit datum, temporarily stores the 1-bit datum, and transmits the 1-bit datum for normal operation; and a non-volatile memory unit (fig. 8, 320), which connects to the SRAM unit for storing the 1-but datum in the SRAM unit before power is turned off (storage operation), keeping the 1-bit datum (storage operation), recovering the 1-bit datum back

to the SRAM unit once the power supply is resumed (recovery operation), and erasing the 1-bit after the recovery operation is completed (erase operation) (col. 1, line 36-62).

With regard to claim 2, Ratnakumar discloses wherein the SRAM unit further comprise a pair of inverters (fig. 8, N1, N2, P1, P2) and two n-channel metal oxide semiconductor field effect transistors (nMOSFET's) (fig. 8, T1, T2), the gates of the nMOSFET's connecting to a word line (fig. 1, WL).

With regard to claim 9, Ratnakumar discloses a non-volatile static random access memory (SRAM) cell, comprising: an SRAM unit (fig. 8, 310), which comprises a first transistor (fig. 8, N1), a second transistor (fig. 8, N2), a third transistor (fig. 8, P1), a fourth transistor (fig. 8, P1), a fifth transistor (fig. 8, T1), and a sixth transistor (fig. 8, T2), wherein the first transistor (fig. 8, N1) and the third transistor (fig. 8, P1) form a first inverter, the second (fig. 8, N2) and the fourth (fig. 8, P2) forms a second inverter, the gates of the first transistor and the third transistor are connected (fig. 8, VD1) to the drains of the fourth transistor and the sixth transistor (fig. 8, VD2), the gates of the second transistor and the fourth transistor are connected to the drains of the first transistor, the third transistor, and the fifth transistor, and the gates of the fifth transistor and the sixth transistor are connected with a word line (fig. 8, VWL); and a non-voltage memory unit (fig. 8, 320), which connects to the SRAM unit (fig. 8, 310) and comprise a seventh transistor (fig. 8, FG1) and an eight transistor (fig. 8, FG2), wherein the gates of the seventh transistor (fig. 8, FG1) and the eighth transistor (fig. 8, FG2) are connected (fig. 8, to voltage terminal VCD), the drain of the seventh transistor (fig. 8, FG1) and the drains of the first transistor(fig. 8, N1), the third transistor (fig. 8, P1), and the fifth

transistor (fig. 8, T1) are connected, and the eighth transistor (fig. 8, FG2)is connected to the drains of the second transistor (fig. 8, N2), the fourth transistor (fig. 8, P2), and the sixth transistor (fig. 8, T2); wherein the SRAM unit (fig. 8, 310), which receives a 1-bit datum, temporarily stores the 1-bit datum, and transmits the 1-bit datum for normal operation; and a non-volatile memory unit (fig. 8, 320), which connects to the SRAM unit for storing the 1-but datum in the SRAM unit before power is turned off (storage operation), keeping the 1-bit datum (storage operation), recovering the 1-bit datum back to the SRAM unit once the power supply is resumed (recovery operation), and erasing the 1-bit after the recovery operation is completed (erase operation) (col. 1, line 36-62).

With regard to claim 10, Ratnakumar discloses wherein the first transistor (fig. 8, N1), the second transistor (fig. 8, N2), the fifth transistor (fig. 8, T1), and the sixth transistor (fig. 8, T2) are nMOSFET's. the third transistor (fig. 8, P1) and the fourth transistor (fig. 8, P2) are pMOSFET's.

Claim Rejections - 35 USC ∋ 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3-8, 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ratnakumar et al, Pat. No. 6556487 in view of Nojima, Pat. No. 6222765.

With regard to claim 3 and 11, Ratnakumar, as applied in prior rejection, disclosed all claimed subject matter except wherein the non-volatile memory unit further comprises two split-gate transistors. However, Nojima discloses a volatile SRAM and non-volatile memory circuit, wherein the non-volatile memory cell section of the circuit comprises a pair of split gate floating gate memory cells (fig. 1, 40 and 54). Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to recognized that the nonvolatile memory unit of Ratnakumar's can be replaced with such pair of split-gate transistors type in Nojima's to use as a non-volatile storage device to store data that is capable of retaining stored charges thereon for an extended period of time without being continuously energized (for example, data will not be lost when power is turned off).

With regard to claim 4, as far as understood, Ratnakumar not discloses the voltage on the control gate of the split-gate transistors is negative and their sources have a high voltage greater than 5V during the erase operation. However, it is well known in the semiconductor art that in a nonvolatile memory erase, or program operation, electrons are normally pulled out of the floating gate or they are being discharged by the electrical field effect. During the period of erasure, the holes produced by band-to-band tunneling current are accelerated by the lateral electrical field and become hot holes. Applying a balance voltage (either increase or decrease, negative or positive or zero or floating) to the source, drain and gate terminal of a memory cell will reduce or increase the lateral electrical field, so as to diminish or increase the acceleration of holes according to the device intended use. Therefore,

appropriate adjusted gate voltage, drain voltage and source voltage and their relative relationship between them are called by the requirements of the circuit based on its intended use (also with regard to claim 5-8, and 12-16).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicants disclosure. Miwa (6285575), Han et al (6064590), Hirose et al (5892712) disclose a memory device having volatile and nonvolatile memory cells.

9. When responding to the office action, Applicants= are advised to provide the examiner with the line numbers and page numbers in the application and/or references' cited to assist the examiner to locate the appropriate paragraphs.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

February 2005

CONNIE C. YOHA
PRIMARY EXAMINER